This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1-7 (canceled)

8. (original) A method of manufacturing a memory structure comprising the steps of:

a) providing a semiconductor substrate;

b) forming a plurality of bottom electrodes;

c) depositing an isolation material overlying the bottom electrodes;

d) etching an opening to the bottom electrodes;

e) depositing a layer of perovskite material overlying the bottom electrodes and the isolation material;

f) polishing the layer of perovskite material, whereby perovskite material remains in the openings to form resistive bits, and

g) forming a plurality of top electrodes overlying the layer of perovskite material.

9. (original) The method of claim 8, wherein the bottom electrodes comprise a bottom electrode material that allows for epitaxial formation of the layer of perovskite material overlying the bottom electrodes.

10. (original) The method of claim 9, wherein the bottom electrode material is YBCO.

11. (original) The method of claim 8, wherein the bottom electrode material is platinum.

12. (original) The method of claim 8, wherein the isolation material is silicon dioxide.

13. (original) The method of claim 8, wherein the perovskite material is a colossal magnetoresistance (CMR) material.

14. (original) The method of claim 8, wherein the perovskite material is $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO).

15. (original) The method of claim 8, wherein the perovskite material is $Gd_{0.7}Ca_{0.3}BaCo_2O_{5+5}$.

16. (original) The method of claim 8, wherein the step of polishing the perovskite material comprises chemical mechanical polishing.

17. (original) The method of claim 8, wherein the top electrodes overly the bottom electrodes forming a cross-point memory configuration.

18. (original) The method of claim 8, further comprising forming a memory circuit prior to depositing the layer of perovskite material.

19. (original) The method of claim 18, wherein the memory circuit comprises a bit pass transistor connected to an input of an inverter and a load transistor connected between the input of the inverter and ground.

20. (original) The method of claim 19, wherein the bit pass transistor is an n-channel transistor and the load transistor is an n-channel transistor.